VLSI Architectures (Sem-2: AY 2024-25)

Lab-7

Objectives:

To add a new instruction “AADD Rx, Ry” to the Min Processor design whose Verilog RTL model was provided to you for study, debugging and simulation in Lab-6. Please refer to the augmented ISA document of the Min processor which incorporates the AADD Rx, Ry instruction which is provided to you for the current lab. exercise (Lab-7) along with Level-II flowchart of AADD Rx, Ry instruction.

The functional description of “AADD Rx, Ry” instruction is provided below:

A new machine language instruction “AADD Rx, Ry” is to be implemented on the Min Execution Unit. This instruction adds all the elements of an array in the memory and returns the result in register Rx. Register Ry contains the memory address of the starting element of the array. Successive elements of the array are in successively increasing memory addresses. An element with numerical value zero serves as the last element of the array. On completion of the instruction execution Rx register contains the sum of all the elements of the array and register Ry contains the memory address of the last element of the array.

Expectation:

1. Please edit the various Verilog modules provided to you as parts of Lab-6 as necessary and add any extra module, if required
2. Write a new test bench to test only this newly added instruction by initializing the PC to zero and storing the AADD Rx, Ry instruction at memory address zero (using register no. 3 as Rx register which contains an initial value 1 and using register no. 4 as Ry register which contains the initial value 10 (which is the starting address of the array in the memory)
3. The array in the memory starts at memory address 10 and it has the following consecutive array element values in the consecutive memory locations: 4, 6, 10, 0